REMARKS

The present amendment is being filed in conjunction with a Request for Continued Examination, and attempts to address the issues raised in an Official Action made final, dated February 24, 2004, wherein the Examiner rejected pending claims 1, 5-16, 29 and 31-34. More specifically, claims 1, 5-7 and 12 are rejected as being anticipated by Chauvel et al., US Patent No. 6,321,299; claims 1, 5-14, 29 and 31-34 are rejected as being anticipated by Chauvel et al., US Patent No. 6,412,048; claims 1, 5-16, 29 and 31-34 are rejected as being anticipated by Yokoyama et al., US Patent No. 5,678,060; and claims 15 and 16 are rejected as being unpatentable over Chauvel et al., '048, in view of Kamiya, US Patent No. 5,809,335. In the present amendment, claims 1, 9, 12, 29 and 31 have been amended, and claims 38-41 have been added.

As presently amended, the claims highlight a data transfer system and corresponding method having a direct memory access element including multiple data busses or interfaces, associated with multiple memories and or processors, and a plurality of nodes, which in at least some embodiments are associated with a plurality of peripherals. The direct memory access element is programmable and/or is adapted for configuring direct memory access data channels to enable the transfer of data between the plurality of nodes and, respectively, the elements associated with the multiple interfaces and/or data busses. None of the references cited teach or suggest the use of a programmable and/or configurable direct memory access system, which provides reconfigurable direct access between at least three groupings of elements including at least one grouping comprising a plurality of nodes.

Specifically, relative to Chauvel et al., '299, the Examiner attempts to identify cache memories which form parts of the corresponding host processor 12 and DSP core 14a, as being equivalent to the claimed first and second memories (claim 1). However, to the extent that the cache memory elements specifically form a part of the respective processor, the corresponding cache memories can not fairly be said to be associated with the corresponding processor, through a shared bus. To the extent that the Examiner alternatively attempts to equate the SDRAM 24 and the Flash 26, as satisfying the claimed first and second memories, these memory elements similarly fail to be associated with a corresponding processor through a shared bus.

Relative to claim 9 and 12 and Chauvel et al., '299, the Examiner has failed to identify a processor (claim 9) coupled to the direct memory access controller ... wherein the processor configures the direct memory access data channel, and/or configuring code (claim 12), which establishes a direct memory access data transfer channel.

Concerning Chauvel et al., '048, relative to claim 1, similar problems as noted above relative to Chauvel et al., '299, are present, where the reference fails to teach a memory associated with a corresponding processor through a shared bus. Where relative to claims 9 and 12, Chauvel et al., '048, teaches away from a direct memory access data channel between a plurality of nodes and both a first memory and a second memory, where only the host processor is identified as supporting transfers with the flash memory (col. 5, lines 19-30). Relative to claim 29, the Examiner has failed to identify the plurality of registers, and more specifically the channel configuration registers, which are used to establish multiple data transfers.

Concerning Yokoyama et al., '060, the Examiner has failed to identify a plurality of peripheral interfaces and/or a plurality of nodes, as being taught and/or suggested by Yokoyama et al., '060, wherein any direct memory access channels, with the corresponding memories are established with only a single respective ATM controller 60. Still further, only bus 90 facilitates the transfer of data with the ATM controller 60 (col. 5, lines 6-17). The other bus 80 facilitates communication control processing with the microprocessor 10 (col. 5, lines 1-5).

The applicants contend that the claims, as presently amended, are allowable over the prior art of record, for the reasons noted above. Allowance of the application is therefore respectfully requested. Should any issues remain unresolved after the consideration of the present response, the Examiner is invited to contact the applicant's representative at the number listed below to discuss the same.

Respectfully submitted,

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